

CBCS Scheme



15CS32

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Third Semester B.E. Degree Examination, Dec.2017/Jan.2018 Analog and Digital Electronics (ADE)

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- Explain the operation and characteristics of N-channel JFET. (08 Marks)
 - With block diagram, explain the operation of a Astable multivibrator using IC 555. (08 Marks)

OR

- With circuit diagram, explain the operation of a Relaxation oscillator. (06 Marks)
 - Fig. Q2(b), shows a Biasing configuration using DEMOSFET given that the saturation drain current is 8mA and the pinch off voltage is -2V.

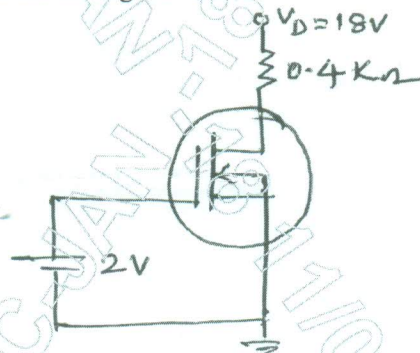


Fig. Q2(b)

- Determine the value of gate source voltage drain current of drain source voltage. (06 Marks)
 - Write the advantages of MOSFET over JFET. (04 Marks)

Module-2

- Give the simplest logic circuit for following logic equation where d represents don't care condition for following locations:
 $F(A, B, C, D) = \sum m(7) + d(10, 11, 12, 13, 14, 15)$. (06 Marks)
 - Simplify the following Boolean function by using Quine – McClusky method.
 $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$. (10 Marks)

OR

- What are Hazards? Explain the types of Hazards and it covers. (08 Marks)
 - Discuss Briefly an HDL Implementation models. (04 Marks)
 - Explain the concept of Duality in Digital circuits. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.



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Module-3

- 5 a. What is multiplexer? Design a 32:1 multiplexer using 16:1 MUX and one 2:1 multiplexer. (05 Marks)
- b. Show how using a 3 to 8 Decoder and multi input OR Gates following Boolean Expressions can be realized simultaneously. (06 Marks)
- $F(A, B, C) = \sum m(0, 4, 6)$
 $F(A, B, C) = \sum m(1, 2, 3, 7)$
 $F(A, B, C) = \sum m(0, 5)$
- c. Show how two 1 to 16 DEMUX can be connected to get 1 to 32 DEMUX. (05 Marks)

OR

- 6 a. Explain parity Generators and checkers using suitable examples. (05 Marks)
- b. What is Magnitude Comparator? Explain 1 bit magnitude comparator. (05 Marks)
- c. What is PLA? Design seven segment Display using PLA. (06 Marks)

Module-4

- 7 a. Explain 4 bit serial in parallel out register. (04 Marks)
- b. Explain a 3 bit binary Ripple up counter. Give the block diagram, truth table and output waveforms. (06 Marks)
- c. Explain the working of JK master slave Flip Flop along with implementation using NAND Gates. (06 Marks)

OR

- 8 a. Design synchronous MOD - 6 counter with truth table and state diagram. (06 Marks)
- b. What is universal shift Register? Explain any one application of universal shift register with block diagram and truth table. (06 Marks)
- c. Write the comparison between Synchronous and Asynchronous counter. (04 Marks)

Module-5

- 9 a. Explain 5 bit Resistive divider with diagram. (06 Marks)
- b. Explain with neat diagram the working principle of Digital clock. (05 Marks)
- c. Explain the terms Accuracy and Resolution for D/A converter. (05 Marks)

OR

- 10 a. Explain with Block diagram the operation of successive approximation converter. (08 Marks)
- b. Explain counter type A/D converter with diagram. (08 Marks)
